Shreesha G. Bhat

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Research Interests

Distributed Systems, Storage Systems, Operating Systems, Networking

Education

University of Illinois Urbana-Champaign 2023 - 2028 (expected)
PhD in Computer Science | Advisors: Ram Alagappan, Aishwarya Ganesan | ***CGPA: 4.0/4.0***

Indian Institute of Technology, Madras 2018 - 2023
Dual Degree (BTech + MTech) in Computer Science & Engineering | Advisor: Kartik Nagar | ***CGPA: 9.66/10.00***

Publications

FMCAD '23 Automating Cutoff-based Verification of Distributed Protocols
Shreesha G. Bhat, Kartik Nagar
Formal Methods in Computer-Aided Design (FMCAD) 2023

DISC '21 Brief Announcement: Automating and Mechanising Cutoff Proofs for Parameterized Verification of Distributed Protocols
Shreesha G. Bhat, Kartik Nagar
35th International Symposium on Distributed Computing (DISC) 2021

Research Experience

Memory Disaggregation | DASSL Lab, UIUC *Aug '23 – present*
Research Assistant | Guide: Ram Alagappan, Aishwarya Ganesan

· Designing and building high-performance systems that leverage networking technologies like RDMA to access un-utilized remote memory to improve memory utilization in modern data centers

Improving Cloud Reliability through Systematic Testing | Microsoft Research India *Aug '22 – Jul '23*
Research Intern | Guide: Akash Lal

· Worked on improving reliability of Azure Cloud Services using concurrency testing tools such as Coyote for C++ programs.
· Built a deterministic concurrency testing framework for a production scale replication library, Azure RSL, which provides an implementation of the Paxos consensus algorithm. Implemented several optimizations to improve state-space coverage.

Parameterized Verification of Distributed Protocols | IIT Madras *Sep '20 – Jul '23*
Young Research Fellow | Guide: Kartik Nagar

· Investigated cutoff-based techniques for verifying that distributed protocols meet their specification irrespective of the size of the parameter they are instantiated with (such as number of nodes).
· Proposed a framework to mechanize simulation based proofs for cutoffs and applied the approach on a variety of distributed protocols using Z3 as a backend SMT solver.

Investigating the FreeBSD Virtual Memory Subsystem | HexHive Lab, EPFL *June '21 - July '21*
Research Intern | Guide: Mathias Payer

· Investigated the FreeBSD boot-up process from a virtual memory management perspective and identified the various mappings and underlying design choices.

Scholastic Achievements

· Secured prizes for excellent academic performance in the 1st, 2nd, 7th and 8th semesters at IIT Madras.
· Secured All India Rank of **851** and **619** in JEE (Joint Entrance Examination) Advanced & Mains 2018
· Qualified for KVPY fellowship with an All India Rank of **142**
· Selected as a undergraduate research fellow as part of the (YRF) program
· Among the **top 300** in India qualified to write national olympiad examinations for Physics, Chemistry and Astronomy (INPhO, INChO, INAO)

Skills

· **Languages** C, C++, Python, Golang, OCaml
· **Tools & Frameworks** RDMA, Z3, LaTeX, Git